IN THE CLAIMS

Please amend the claims as follows:

1(Currently amended). A reconfigurable chip including:

first and second multiplication units ~~multiplexers~~; and

a first multiplexer selectively connectable to supply first and second operands, where in a first configuration the first operand is supplied through a second multiplexer to a first input of the first multiplication unit and the second operand is supplied through a third multiplexer to a first input of the second multiplication unit.

~~a multiplication block including a first multiplication unit and an adder unit selectively connectable in different configurations, a first configuration coupling first and second inputs of the first multiplication unit to outputs of the first and second multiplexers to receive first and second operands, and a second configuration coupling first and second inputs of the adder unit respectively to the outputs of the first and second multiplexers to receive the first and second operands.~~

2(Currently amended). The reconfigurable chip of claim 1 further including: ~~wherein the first and second configurations are selected by an instruction supplied to the multiplication block.~~

a fourth multiplexer selectively connectable to supply third and fourth operands, where in the first configuration the third operand is supplied through a fifth multiplexer to a second input of the first multiplication unit and the fourth operand is supplied through a sixth multiplexer to a second input of the second multiplication unit.

3(Currently amended). The reconfigurable chip of claim 2, further including an adder unit having first and second inputs respectively coupled to outputs of the first and second multiplication units ~~a second multiplication unit having first and second inputs coupled to outputs of the first and second multiplexers~~.

4(Currently amended). The reconfigurable chip of claim 3, wherein the first and second inputs of the adder unit are coupled through seventh and eighth multiplexers to the outputs of the first and second multiplication units ~~further including a third configuration with the adder unit having first and second inputs respectively coupled to outputs of the first and second multiplication units.~~

Claims 5-17 (Canceled).

18(Currently amended). A reconfigurable chip including:

a multiplication block including first and second multiplexers, a multiplication unit having first and second multipliers ~~inputs~~, and ~~first and second~~ an adder ~~units~~ unit, wherein a first configuration instruction to the multiplication block configures the multiplication unit to receive ~~first and second~~ operands from the first and second multiplexers and provide a summed product of the operands at an output, and a second configuration instruction configures the ~~first and second~~ adder ~~units~~ unit to receive the ~~first and second~~ operands from the first and second multiplexers and provide a summed value of the operands.